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First Named Inventor	Setsuo NAKAJIMA et al.
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ENCLOSURES *(check all that apply)*

- ☐ Fee Transmittal Form
  - ☐ Fee Attached
- ☐ Amendment / Reply
  - ☐ After Final
  - ☐ Affidavits/declaration(s)
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- ☐ Status Letter
- ☒ Other Enclosures
  1. Submission of Verification of Translation
  2. JP 09-205345 filed 07/14/1997
  3.
  4.
  5.
  6.

Remarks

☒ The Commissioner is hereby authorized to charge any additional fees required or credit any overpayments to Deposit Account No. 50-2280 for the above identified docket number.

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date indicated below.

Type or printed name	Adele M Stamper		
Signature	Adele M Stamper	Date	10-19-05

Attorney Docket No. 0756-7220

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:	)	Group Art Unit: 2813
Setsuo NAKAJIMA et al.	)	Examiner: T. Ngueyn
Serial No. 10/706,986	)	CERTIFICATE OF MAILING
Filed: November 14, 2003	)	I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on 10-19-05.
For: METHOD OF FABRICATING SEMICONDUCTOR DEVICE	)	Adela M Stamper

SUBMISSION OF VERIFICATION OF TRANSLATION

Honorable Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Further to the Amendment filed on August 9, 2005, Applicant submits herewith a verified English translation of priority Japanese Application No. 09-205345 filed July 14, 1997.

Applicant respectfully submits that the 102(e) rejection has been overcome with the submission of the verified English translation. Reconsideration and withdrawal of the rejection under 102(e) is requested.

Respectfully submitted,

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Docket No.: 0756-7220

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:	)	
Setsuo NAKAJIMA et al.	)	
Application No.: 10/706,986	)	Art Unit: 2813
Filed: November 14, 2003	)	Examiner: T. Ngueyn
For: METHOD OF FABRICATING SEMICONDUTOR DEVICE	)	

VERIFICATION OF TRANSLATION

Honorable Commissioner of Patents and Trademarks

P.O. Box 1450

Alexandria, VA 22313-1450

Sir:

I, Maki Shinohara, 710-1-510, Ishida, Isehara-shi, Kanagawa-ken 259-1116 Japan, a translator, herewith declare:

that I am well acquainted with both the Japanese and English Languages;

that I am the translator of the attached translation of the Japanese Patent Application No. 9-205345 filed on July 14, 1997; and

that to the best of my knowledge and belief the followings is a true and correct translation of the Japanese Patent Application No. 9-205345 filed on July 14, 1997.

I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Date: this 12th day of October 2005

Maki Shinohara

Name: Maki Shinohara

[Name of Document] Patent Application

[Reference Number] P003674-02

[Filing Date] July 14, 1997

[Attention] Commissioner, Patent Office

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[Title of the Invention] METHOD FOR MANUFACTURING A SEMICONDUCTOR DEVICE

[The Number of Claims] 12

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[List of Attachment]

[Attachment] Specification 1

[Attachment] Drawing 1

[Attachment] Abstract 1

[Name of Document] Specification

[Title of the Invention] METHOD FOR MANUFACTURING A SEMICONDUCTOR DEVICE

[Scope of Claim]

[Claim 1]

A method for manufacturing a semiconductor device characterized by comprising the steps of:

forming a silicon film crystallized by a function of a metal element for promoting crystallization of silicon;

forming a mask which exposes a part of the silicon film;

forming a film containing an element belonging to group 15 of periodic table covering the mask and the part of the exposed silicon film; and

performing heat treatment and moving the metal element from the silicon film to the film containing the element belonging to group 15 of periodic table.

[Claim 2]

A method for manufacturing a semiconductor device characterized by comprising the steps of:

forming a silicon film crystallized by a function of a metal element for promoting crystallization of silicon;

forming a mask which exposes a part of the silicon film;

forming a film containing an element belonging to group 15 of periodic table covering the mask and the part of the exposed silicon film; and

performing heat treatment and gettering the metal element from the silicon film to the film containing the element belonging to group 15 of periodic table.

[Claim 3]

A method for manufacturing a semiconductor device characterized by comprising the steps of:

forming a mask over an amorphous silicon film to expose a part thereof;

introducing selectively a metal element for promoting crystallization of silicon into the part of region in which the amorphous silicon film is exposed;

performing heat treatment and diffusing the metal element from the part of the region into a silicon film;

forming a silicon film containing in the part of the region an element belonging to group 15 of periodic table over the mask and contacting the silicon film containing the element belonging to group 15 of periodic table with the silicon film in which the metal element is diffused; and

performing heat treatment and moving the metal element from the silicon film in which the metal element is diffused into the silicon film containing the element belonging to group 15 of periodic table through the part of the region.

[Claim 4]

A method for manufacturing a semiconductor device characterized by comprising the steps of:

forming a mask over an amorphous silicon film to expose a part thereof;

introducing selectively a metal element for promoting crystallization of silicon into the part of region in which the amorphous silicon film is exposed;

performing heat treatment and diffusing the metal element from the part of the region into a silicon film;

forming a silicon film containing in the part of the region an element belonging to group 15 of periodic table over the mask and contacting the silicon film containing the element belonging to group 15 of periodic table with the silicon film in which the metal element is diffused; and

performing heat treatment and gettering the metal element from the silicon film in which the metal element is diffused into the silicon film containing the element belonging to group 15 of periodic table through the part of the region.

[Claim 5]

The method for manufacturing a semiconductor device according to claims 1 to 4 characterized by using one kind or a plurality of kinds of elements selected from Fe, Co, Ni, Ru, Rh, Pd, Os, Ir, Pt, Cu, Au, Ge, Pb, and In as a metal element for promoting crystallization of silicon.

[Claim 6]

The method for manufacturing a semiconductor device according to claims 1 to 4 characterized by using P as the element belonging to group 15 of periodic table.

[Claim 7]

The method for manufacturing a semiconductor device according to claims 1 to 4 characterized by using an element selected from P, As, and Sb as the element belonging to group 15 of periodic table.

[Claim 8]

The method for manufacturing a semiconductor device according to claims 1 to 4 characterized by comprising a step of irradiating the silicon film containing the element belonging to group 15 of periodic table element with laser light or strong light and activating phosphorus.

[Claim 9]

The method for manufacturing a semiconductor device according to claims 1 to 4 characterized by performing heat treatment with a resistance heating-type furnace.

[Claim 10]

The method for manufacturing a semiconductor device according to claims 1 to 4 characterized by performing heat treatment by strong light irradiation.

[Claim 11]

The method for manufacturing a semiconductor device according to claims 1 to 4 characterized by using nickel as the metal element for promoting crystallization of silicon, and using P (phosphorus) as the element belonging to group 15 of periodic table element.

[Claim 12]

The method for manufacturing a semiconductor device according to claims 1 to 4 characterized by performing a second heat treatment step at temperature obtained by a temperature range from 600 to 750°C.

[Detailed Description of the Invention]

[0001]

[Technical Field to which the Invention pertains]

The present invention disclosed in this specification relates to a method for manufacturing a thin film transistor using a crystalline silicon film.

[0002]

[Prior Art]

A thin film transistor (hereinafter referred to as a TFT) using a silicon thin film in an active layer is known. The TFT is mainly put to practical use in an active matrix liquid crystal display device.

[0003]

The thin film transistor currently put to practical use has a so-called a-Si TFT using an amorphous silicon film and a so-called high-temperature p-Si TFT using a normal IC process.

[0004]

High-temperature p-Si is obtained by using a technique for obtaining a crystalline silicon film by using heat treatment at a high temperature such as 900°C or higher.

[0005]

In terms of requiring a high characteristic, it is preferable to use a crystalline silicon film. However, at a heat treatment temperature necessary for manufacturing a high-temperature p-Si film, there is a problem in that a glass substrate cannot be used as a substrate.

[0006]

The thin film transistor is mainly used in an LCD device and required to be able to use a glass substrate as a substrate.

[0007]

As a means for solving this problem, research has been conducted into a technique for manufacturing a crystalline silicon film by a process at a temperature (this temperature is conveniently referred to as a low temperature) that the glass substrate can withstand.

[0008]

This process is referred to as a low-temperature process corresponding to a

process (high-temperature processes) for manufacturing the high-temperature p-Si. Further, a crystalline silicon film manufactured by this low-temperature process is referred to as a low-temperature p-Si, and a TFT using a low-temperature p-Si film is referred to as a low-temperature p-Si TFT.

[0009]

A technique for manufacturing a low-temperature p-Si film can be roughly classified into a method by laser irradiation and a method by heating.

[0010]

The method by laser irradiation is characterized in that it gives little thermal damage to the glass substrate because the laser light is directly absorbed near the surface of the amorphous silicon film.

[0011]

However, there is a problem in stability of a laser oscillator and there is also a problem in an application to a large area.

[0012]

On the other hand, a current situation is that the method by heating cannot provide a required crystalline silicon film by heat treatment at a temperature to which the glass substrate can withstand.

[0013]

There is a technique disclosed in Japanese Patent Laid-Open No. Hei 6-268212 as a technique for improving such existing problems.

[0014]

In this technique, a metal element for promoting crystallization of silicon, typified by nickel, is maintained in contact with the surface of an amorphous silicon film. Thereafter, heat treatment is performed. Thus, a crystalline silicon film having required crystallinity can be obtained at a temperature which is lower than the conventional temperature and which the glass substrate withstands.

[0015]

This crystallization technique using nickel is useful in that a crystalline silicon film having required crystallinity can be obtained by heat treatment conducted at a

temperature low enough that the glass substrate can withstand.

[0016]

However, nickel used for the crystallization inevitably remains in the active layer. This leads to instability of the characteristics of the TFT and deterioration of reliability.

[0017]

[Problems to be Solved by the Invention]

The invention disclosed in this specification is to provide a configuration to eliminate an effect of a nickel element remaining in the obtained silicon film in the technique to obtain a crystalline silicon film using the aforementioned metal element for promoting crystallization of silicon.

[0018]

[Means for Solving the Problem]

One of the invention disclosed in this specification is, as shown in one example of the manufacturing steps in FIG. 1, a method for manufacturing a semiconductor device characterized by comprising the steps of forming a silicon film 104 crystallized by a function of a metal element (such as nickel) for promoting crystallization of silicon; forming a mask 105 which exposes a part of the silicon film; forming a film 106 containing an element belonging to group 15 of periodic table element (such as phosphorus) covering the mask 105 and the part of the exposed silicon film 104; and performing heat treatment and moving the metal element from the silicon film 104 to the film 106 containing the element belonging to group 15 of periodic table element (FIG. 1 (D)).

[0019]

In the aforementioned configuration, as for the nickel element which moves by heat treatment, it can be said that the silicon films 104 and 106 are combined. That is, for the nickel element which moves by heat treatment, the silicon films 104 and 106 are not be distinguished specifically.

[0020]

Accordingly, in the heat treatment step shown in FIG. 1 (D), the nickel element

contained in the silicon film 104 is diffused into the silicon film 106. Note that the metal element is hardly diffused into a silicon oxide film 105.

[0021]

On the other hand, the silicon film 106 contains phosphorus which serves as a gettering site for nickel at high concentration. Therefore, the nickel element which moves into the silicon film 106 bonds with phosphorus and stabilized.

[0022]

If a heat treatment temperature in FIG. 1 (D) is set at 800°C or lower, or preferably 750°C or lower, phosphorus is hardly diffused through the silicon film and nickel once taken in the silicon film 106 remains there. The nickel is not diffused back into the silicon film 104.

[0023]

In this way, the nickel element in the silicon film 104 moves into the silicon film 106. It can be said that the nickel element in the silicon film 104 is gettered into the silicon film 106.

[0024]

During the heat treatment in a state shown in FIG. 1 (D), the whole silicon film 106 acts as a gettering site. Therefore, even if a contact area between the silicon film 104 and the silicon film 106 is relatively small, nickel can move effectively. That is, the nickel element in the silicon film 104 can be effectively reduced.

[0025]

Another configuration of the invention is, as shown in a specific example in FIG. 3, a method for manufacturing a semiconductor device characterized by comprising the steps of: forming a mask 302 over an amorphous silicon film 301 and a part thereof is exposed by an opening portion 303 formed in the mask; introducing selectively a metal element for promoting crystallization of silicon into the part of region in which the amorphous silicon film is exposed (FIG. 3 (B)); performing heat treatment and diffusing the metal element from the part of the region into a silicon film (FIG. 3 (C)); forming a silicon film 307 containing phosphorus over the mask 302 and contacting the silicon film containing phosphorus with a silicon film in which the metal element is diffused in

the part of the region (FIG. 3 (D)); and performing heat treatment and moving the metal element from the silicon film in which the metal element is diffused into the film containing phosphorus through the part of the region as indicated by an arrow 308 (FIG. 3 (D)).

[0026]

In the case of adopting the aforementioned configuration, nickel can be removed from the region in which the metal element is introduced (the region forming the opening 303), by using the mask 302 to induce crystal growth, referred to as lateral growth, as shown in FIG. 3 (C). Since the same mask pattern can be used both for the introduction of the metal element and for the removal of the metal element, the configuration has an advantage that the step is not complicated so much.

[0027]

During the nickel-removing step shown in FIG. 3 (D), an area of the silicon film 307 is far larger than that of the opening portion 303. Therefore, in the process that the nickel element is diffused into a majority of the silicon film 307, the nickel element is effectively gettered from a part of the opening portion 303 in the mask to the silicon film 307.

[0028]

Use of nickel is the most preferred as the metal element for promoting crystallization of silicon. Further, use of P (phosphorus) is the most preferred as the element belonging to group 15 of periodic table element. That is, in the case where a combination of nickel and phosphorus is adopted, the highest effect of the invention can be obtained.

[0029]

One or a plurality of elements selected from Fe, Co, Ni, Ru, Rh, Pd, Os, Ir, Pt, Cu, Au, Ge, Pb, and In can be used as the metal element for promoting crystallization of silicon.

[0030]

Further, an element selected from P, As, or Sb can be used as the element belonging to group 15 of periodic table element.

[0031]

[Embodiment Modes of the Invention]

As illustrated in a specific example in FIG. 1, nickel is maintained in contact with a surface of the amorphous silicon film as indicated by reference numeral 103. Thereafter, heat treatment is performed at 600°C for eight hours to crystallize an amorphous silicon film 102. In this way, the crystalline silicon film 104 is obtained.

[0032]

As for method for introducing Ni, a method using a solution is easy to use and introduced amount can be readily adjusted. Besides the method using the solution, CVD, sputtering, evaporation, gas adsorption, ion implantation and the like can be used. Whatever the method may be, as for the method for introducing nickel, a state that the nickel element is maintained in contact with the surface of the amorphous silicon film or a state that the nickel element is present in the amorphous silicon film may be realized. This is the same even as a case where a metal element other than nickel is used.

[0033]

Thereafter, the mask 105 formed of a silicon oxide film is formed, and further the amorphous silicon film 106 doped with phosphorus at high concentration is formed. Then, heat treatment is performed to getter the nickel element from the crystalline silicon film 104 to the amorphous silicon film 106.

[0034]

In the invention disclosed in this specification, the film 104 in which gettering is performed and the film 106 which performs gettering are formed of the same silicon film. Consequently, the nickel element can be effectively moved. That is, nickel can be effectively gettered.

[0035]

[Embodiments]

[Embodiment 1]

In this embodiment, an example of a case where an N-channel TFT is manufactured is shown. First, a silicon oxide film 100 is formed as a base film over a

glass substrate 101 with a thickness of 300 nm by plasma CVD. (FIG. 1 (A))

[0036]

Here, a Corning 1737 substrate (a strain point of 667°C) is used as the glass substrate.

[0037]

After forming the base film, the amorphous silicon film 102 is formed with a thickness of 50 nm by plasma CVD.

[0038]

As for a method for forming an amorphous silicon film, low pressure thermal CVD is the most preferred, though herein, plasma CVD with high productivity is used.

[0039]

After forming the amorphous silicon film 102, a nickel acetate solution which is adjusted at a concentration of 10 ppm by weight conversion is coated, and a state in which the nickel element is maintained in contact with the surface as indicated by reference numeral 103 is obtained.

[0040]

Thus, the state shown in FIG. 1 (A) is obtained. Next, as shown in FIG. 1 (B), the mask 105 formed of the silicon oxide film is formed. Here, the thickness of the silicon oxide film forming the mask 105 is 250 nm. As for a material for forming the mask 105, a silicon nitride film or a silicon oxynitride film can be selected.

[0041]

Next, the amorphous silicon film 106 doped with phosphorus at high concentration is formed by plasma CVD. Here, 97% by volume of silane and 3% by volume of phosphine are used as source gas, and the amorphous silicon film 106 is formed with a thickness of 150 nm.

[0042]

As for a film forming method, low pressure thermal CVD may be used. Alternatively, a microcrystalline silicon film may be formed by setting film forming conditions.

[0043]

Phosphorus doping is set with conditions that the concentration of phosphorus in the formed amorphous silicon film is 1×10^{19} atoms/cm^3 or higher, preferably 5×10^{19} atoms/cm^3 higher. Phosphorus is doped to getter nickel later.

[0044]

After forming the amorphous silicon film 106 as shown in FIG. 1 (C), heat treatment is performed. Here, heat treatment is carried out at 600°C for eight hours in a nitrogen atmosphere. During this step, the nickel element moves from the crystalline silicon film 104 into the amorphous silicon film 106 as indicated by an arrow of FIG. 1 (D). This effect can be obtained in the case where quite a thin oxide film (approximately 10 nm or less) or a natural oxide film is formed on the surface of the crystalline silicon film 104.

[0045]

This is due to that the nickel element is diffused very actively, and phosphorus and nickel have various binding states and the binding states are very stable.

[0046]

A heat treatment temperature is selected in the range from 450 to 750°C (substantially limited by a strain point of the glass substrate). To enhance a gettering effect, it is preferred to select from higher temperature.

[0047]

If a heat treatment temperature is lower than the aforementioned range, the diffusion velocity and the diffusion distance of nickel are insufficient and gettering effect is not obtained sufficiently.

[0048]

On the other hand, if a heat treatment temperature is higher than the aforementioned range, the diffusion velocity and the diffusion distance of nickel are sufficient. However, the diffusion of phosphorus cannot be neglected and an effect to bias nickel in a certain region cannot be obtained.

[0049]

When the heat treatment shown in FIG. 1 (D) is performed, the nickel element is gettered into the amorphous silicon film 106, therein, the nickel element is present at

high concentration.

[0050]

Next, the amorphous silicon film 106 containing the nickel element at high concentration is removed by etching. At this time, the crystalline silicon film 104 in the area to which the mask 105 formed of the silicon oxide film is not provided is also removed at the same time (FIG. 1 (E)).

[0051]

In this way, a crystalline silicon film pattern indicated by reference numeral 107 is formed. This crystalline silicon film pattern is that the crystallization is carried out by once diffusing nickel into the film, thereafter the nickel element is removed to outside of the film during the step shown in FIG. 1 (D).

[0052]

Next, the mask 105 formed of the silicon oxide film is removed. Then, as shown in FIG. 2 (A), a silicon oxide film 108 is formed with a thickness of 120 nm by plasma CVD. This silicon oxide film 108 functions as a gate insulating film.

[0053]

Next, an aluminum film (not shown) for forming a gate electrode is formed with a thickness of 400 nm by sputtering. This aluminum film is formed using a target containing 0.18% by weight of scandium.

[0054]

The aluminum film contains scandium for suppressing formation of barb or needle-like projection called hillock or whisker due to overgrowth of aluminum in later steps.

[0055]

Next, the aluminum film (not shown) is patterned using a resist mask 200 to form a pattern 109 illustrated in FIG. 2 (A).

[0056]

Next, anodization is performed using the aluminum pattern 109 as an anode in the state in which the resist mask 200 is remained.

[0057]

During this step, an aqueous solution containing 3% (volume) of oxalic acid is used as an electrolyte. Current is supplied between both electrodes with the aluminum pattern as an anode and platinum as a cathode. In this way, an anodic oxide film 111 is formed.

[0058]

This step is carried out in the state that the resist mask 200 remains. Therefore, the anodic oxide film indicated by reference numeral 111 is formed on the sides of the aluminum pattern 109. Note that the remaining aluminum film pattern is indicated by reference numeral 110.

[0059]

In this embodiment, the anodic oxide film 111 grows a distance of 400 nm. The anodic oxide film 111 formed in this embodiment is porous (porous state).

[0060]

After forming the anodic oxide film 111, the resist mask 200 is removed. Then, anodic oxidation is performed again. During this step, an electrolyte prepared by neutralizing an ethylene glycol solution containing 3% (volume) of tartaric acid with aqueous ammonia is used.

[0061]

Since the electrolyte enters inside the porous anodic oxide film 111, an anodic oxide film indicated by reference numeral 112 is formed in this step. That is, the anodic oxide film 112 is formed over the surface of the aluminum pattern 110.

[0062]

The thickness of this anodic oxide film 112 is 70 nm. This anodic oxide film has a dense membranous.

[0063]

In this way, a state shown in FIG. 2 (B) is obtained. Here, the remaining aluminum pattern 110 becomes a gate electrode of a TFT.

[0064]

Next, the exposed silicon oxide film 108 is removed, using the gate electrode 110, the anodic oxide film 112 with a dense membranous in the periphery thereof and

the anodic oxide film 112 with a denser membranous as a mask.

[0065]

Here, the exposed silicon oxide film 108 is etched away by dry etching (RIE) having perpendicular anisotropy. In this manner, a state as shown in FIG. 2 (C) is obtained.

[0066]

Next, phosphorus doping is carried out by plasma doping. The plasma doping is a doping method in which source gas containing a dopant element is changed into plasma, dopant ions are extracted therefrom by an electric field, and the extracted ions are accelerated by the electric field and injected into doped regions. Especially, the plasma doping refers to as a method in which mass separation using a magnetic field is not carried out.

[0067]

On the other hand, a method in which mass separation often used in manufacturing ICs and the like is carried out and the divided dopant ions are accelerating injected is referred to as ion implantation.

[0068]

The plasma doping has the advantage corresponding with large areas. However, there is a problem in that other elements such as hydrogen contained in dopant gas are also doped.

[0069]

By this doping, phosphorus doping is carried out into regions 114 and 116. For convenience, these doped regions are referred to as high concentration impurity regions. Note that the regions 114 and 116 become a source region and a drain region respectively later.

[0070]

This doping may be carried out under normal doping conditions for forming source and drain regions.

[0071]

Further, a region indicated by reference numeral 113 remains as an undoped

region.

[0072]

Next, the porous anodic oxide film 111 is removed as shown in (D). Then, phosphorus doping is carried out again by plasma doping. This step is performed at a lower dosage than the doping at the step shown in (C).

[0073]

In this way, low concentration impurity regions 201 and 203 in which doping is carried out at lower dosage than that of the source and drain regions are formed in a self-aligned manner. (FIG. 2 (D))

[0074]

Further, an undoped region 202 is defined as a channel region. (FIG. 2 (D))

[0075]

Next, excimer laser light is irradiated to activate the doped regions. Specifically, the damage to the doped regions caused in the doping is annealed out and the dopant in the doped regions is activated.

[0076]

Note that highly resistive regions are formed adjacent to the channel region 114 with the thickness of the anodic oxide film 112 with a dense membranous. However, in this embodiment, since the thickness of the anodic oxide film 112 is as thin as 70 nm, the presence thereof is neglected.

[0077]

Next, as shown in FIG. 2 (E), a silicon nitride film 116 is formed as an interlayer insulating film with a thickness of 250 nm by plasma CVD. Furthermore, an acrylic resin film 117 is formed by spin coating. The thickness of the acrylic resin film 117 is 700 nm at the thinnest part.

[0078]

Furthermore, a contact hole is formed, and a source electrode 118 and a drain electrode 119 are formed. In this way, a TFT (thin film transistor) as shown in FIG. 2 (E) is completed.

[0079]

The thin film transistor indicated in this embodiment can make the active layer 107 with high crystallinity by using nickel. At the same time, gettering is performed as shown in FIG. 1 (D) to greatly reduce the degree of the nickel element remaining in the active layer 107.

[0080]

Further, crystallization by heat treatment can be performed at a lower temperature than conventionally done (than in the case where no nickel is used). Therefore, an inexpensive glass substrate can be used.

[0081]

[Embodiment 2]

This embodiment is an example of a case where a P-channel TFT is manufactured during the manufacturing step shown in Embodiment 1.

[0082]

For manufacturing the P-channel TFT, boron may be doped instead of phosphorus in the steps shown in FIGS. 2 (C) and 2 (D). The other parts are the same as the manufacturing step shown in Embodiment 1.

[0083]

[Embodiment 3]

This embodiment is an example of a case where a gate electrode is formed of a material other than aluminum during the manufacturing step shown in Embodiment 1. In this embodiment, an example of a case where the gate electrode is formed of tungsten silicide is shown.

[0084]

As for the gate electrode, various silicide materials and various metallic materials in addition to tungsten silicide may be used. Further, a silicon material to which conductivity is imparted can be used as the material for forming the gate electrode. Moreover, a stacked structure of various conductive materials may be adopted as the structure of the gate electrode.

[0085]

Generally, in the case of using aluminum, an advantage of low resistance is

obtained. However, there is a problem in that a process temperature is limited. On the other hand, in the case of using other materials, higher resistance is obtained compared with aluminum, though there is an advantage that relatively higher heat-resistance is obtained and the process temperature can be elevated.

[0086]

[Embodiment 3]

This embodiment is that a step for removing the nickel element (remaining minor amount of nickel element) in the channel region is added in addition to a nickel-gettering process shown in FIG. 1 (D) during the manufacturing step shown in Embodiment 1.

[0087]

By performing the nickel-gettering process shown in FIG. 1 (D), nickel concentration in a region indicated by reference numeral 104 in FIG. 1 (E) decreases to an unmeasurable level.

[0088]

Specifically, the nickel concentration measured immediately after the crystallization by SIMS (method for analyzing secondary ion) is approximately 1×10^{18} atoms/cm^3 to 5×10^{19} atoms/cm^3. The nickel concentration can be reduced to 10^{17} atoms/cm^3 or less by performing the step shown in FIG. 1 (D).

[0089]

That is, the concentration of the nickel element remaining in the region 107 shown in FIG. 1 (E) can be reduced to 10^{17} atoms/cm^3 or lower.

[0090]

Accordingly, the concentration of the nickel element in the active layer in the TFT manufactured through the manufacturing process shown in Embodiment 1 can be 10^{17} atoms/cm^3 or lower.

[0091]

However, in the case where strict demands are made on characteristic variations or reliability, even the aforementioned nickel concentration levels may not be sufficient.

[0092]

According to research by the inventors, what mainly produces an adverse effect on the TFT characteristics is the nickel element present in the active layer, especially in the channel region and near the interfaces between the channel region and the impurity regions.

[0093]

Accordingly, in this embodiment, especially the nickel element remaining in the channel region is to be reduced.

[0094]

In this embodiment, heat treatment is added to the step shown in (D) during the manufacturing step shown in Embodiment 1. This heat treatment is carried out at a temperature of 450°C for two hours.

[0095]

Thus, the nickel element remaining in the channel region 114 is gettered in the source region 114 and the drain region 116 which are high concentration impurity regions. That is, the concentration of the nickel element remaining in the channel region 114 decreases while the concentration of the nickel element in the source region 114 and the drain region 116 increases.

[0096]

Then, the concentration of the nickel element remaining in the channel region reduces and the adverse effect on the TFT characteristics by the remaining nickel can be suppressed.

[0097]

Note that in the case where the gate electrode is changed to a silicide material with higher heat resistance or the like, heat treatment with a higher temperature is effective. For example, in the case where tungsten silicide is used as the gate electrode material and heat treatment is performed at 600°C for two hours as heat treatment, the gettering effect can be obtained more effectively.

[0098]

Further, heat treatment may also be performed at a stage of FIG. 2 (C).

[0099]

In the case of performing the configuration shown in this embodiment, the effect of the nickel element remaining in the source and drain regions is concerned. However, the source and drain regions differ from the channel region in that a change in the conductivity type and resistance change do not occur. Therefore, the presence of nickel does not become a problem especially.

[0100]

[Embodiment 4]

This embodiment shows an example of a case where a crystal growth different from the method of Embodiment 1, especially the method shown in FIG. 1 (A), is performed.

[0101]

A manufacturing step of this embodiment is shown in FIG. 3. In this embodiment, the step up to obtaining an active layer pattern for a TFT is shown.

[0102]

Further, in FIG. 3, the same numerals as those of FIG. 1 are used to show the same portions as those shown in Embodiment 1. Moreover, the places of the reference numerals are the same as Embodiment 1 as long as not noticing a manufacturing condition and the like especially.

[0103]

First, as shown in FIG. 3 (A), the glass substrate 101 is prepared. The silicon oxide film 100 is formed over the glass substrate 101 as a base film with a thickness of 300 nm by plasma CVD.

[0104]

In this embodiment, the Corning 1737 glass substrate is used as the substrate 101.

[0105]

After forming the base film 100, the amorphous silicon film 301 is further formed. Here, the amorphous silicon film 301 is formed with a thickness of 50 nm by low pressure thermal CVD.

[0106]

Next, the mask 302 formed of a silicon oxide film is formed. Here, first, a silicon oxide film (not shown) is formed with a thickness of 120 nm by plasma CVD and the silicon oxide film is patterned to form the mask 302. (FIG. 3 (B))

[0107]

Next, the nickel acetate solution which is adjusted at a nickel concentration of 10 ppm by weight conversion is coated. Thus, a state in which the nickel element is maintained in contact with the exposed surface as indicated by reference numeral 302 is obtained. (FIG. 3 (B))

[0108]

Next, heat treatment is performed at 600°C for eight hours in a nitrogen atmosphere. At this time, the nickel element is diffused into the amorphous silicon film 301 from the region with which the nickel element is in contact. Accordingly, crystallization of the amorphous silicon film 301 progresses in the path as indicated by an arrow 305. (FIG. 3 (C))

[0109]

In this way, a crystalline silicon film 306 having peculiar crystal growth mode is obtained. That is, obtained is the crystalline silicon film 306 of which crystals are grown in a direction parallel to the membrane surface from the opening portion 303 in the mask in which nickel is introduced. In this specification, this crystal growth mode is referred to as lateral growth. Moreover, the region in which this crystal growth is performed is referred to as a lateral-growth region. (FIG. 3 (C))

[0110]

Next, the amorphous silicon film 307 doped with phosphorus at high concentration is formed with a thickness of 300 nm by plasma CVD. (FIG. 3 (D))

[0111]

Next, heat treatment is performed at 600°C for eight hours to getter the nickel element remaining in the crystalline silicon film 104 into the amorphous silicon film 106.

[0112]

That is, heat treatment is performed to incorporate the nickel present in the

silicon film 306 into the phosphorus present in the amorphous silicon film 106. This step is called a step that the nickel element present in the crystalline silicon film 104 is absorbed into the amorphous silicon film 106 containing nickel at high concentration accordingly.

[0113]

Note that during this step, the amorphous silicon film 307 is crystallized, which is not a problem.

[0114]

Next, the silicon film 307 is removed and the silicon film 306 is etched while using the mask 302 formed of the silicon oxide film as a mask. In this way, a silicon film pattern 309 shown in FIG. 3 (E) is obtained.

[0115]

Next, an active layer pattern for a TFT (for example, this pattern corresponds to reference numeral 107 in FIG. 1 (E)) is formed using the lateral growth region in the silicon film pattern 309. Then, the TFT is manufactured in accordance with the manufacturing steps hereinafter FIG. 2 (A) shown in Embodiment 1. It is needless to say that other TFTs may be manufactured using the lateral growth region. Moreover, the configuration shown in Embodiment 2 or 3 can be adopted in addition to the configuration shown in Embodiment 1.

[0116]

[Embodiment 5]

This embodiment shows an example of a case of manufacturing a bottom-gate TFT. The manufacturing step of this embodiment is shown in FIG. 4.

[0117]

First, a gate electrode 402 is formed over a glass substrate 401. In this embodiment, an example of a case where a base film is not formed over the glass substrate is shown. (FIG. 4 (A))

[0118]

The gate electrode 402 is required to select a material capable of withstanding a heat treatment step later. Here, a tantalum film with a thickness of 400 nm formed by

sputtering is used as the gate electrode 402. (FIG. 4 (A))

[0119]

After forming the gate electrode 402, a silicon oxide film 403 to be a gate insulating film is formed with a thickness of 100 nm by plasma CVD.

[0120]

Next, an amorphous silicon film 404 is formed with a thickness of 50 nm by plasma CVD. Note that instead of plasma CVD, low pressure thermal CVD may be used as a forming method of the amorphous silicon film.

[0121]

Next, a nickel acetate solution is coated over the whole surface of the exposed surface of the amorphous silicon film, so that a state in which the nickel element is maintained in contact as indicated by reference numeral 405 is obtained. (FIG. 4 (A))

[0122]

Here, an example in which the nickel element is introduced into the whole surface of the amorphous silicon film is shown, though a configuration in which nickel is selectively introduced providing a mask as shown in FIG. 3 and the lateral growth is performed may be used.

[0123]

Next, heat treatment is performed at 600°C for eight hours to crystallize the amorphous silicon film 404 and to obtain a crystalline silicon film 400. (FIG. 4 (B))

[0124]

Next, a mask 406 formed of a silicon oxide film is formed. Here, a silicon oxide film (not shown) is formed with a thickness of 150 nm by plasma CVD and the silicon oxide film is patterned to form a pattern indicated by reference numeral 406.

[0125]

Next, an amorphous silicon film 407 doped with phosphorus at high concentration is formed with a thickness of 200 nm by plasma CVD.

[0126]

Here, the amorphous silicon film 407 is formed using membrane gas mixed at a ratio of 98% by volume of silane and 2% by volume of phosphine. (FIG. 4 (B))

[0127]

Next, heat treatment is performed at 600°C for four hours in a nitrogen atmosphere. During this step, the nickel element diffused in the silicon film 400 moves into the amorphous silicon film 407 side as indicated by reference numerals 408 and 409. (FIG. 4 (B))

[0128]

Next, the amorphous silicon film 407 containing nickel at high concentration is removed. Furthermore, using the mask 406, a part of the crystalline silicon film 400 (a region which is not provided with the mask 406) is removed. (FIG. 4 (C))

[0129]

In this way, a crystalline silicon film 410 patterned by the mask 406 is obtained. (FIG. 4 (C))

[0130]

In the crystalline silicon film 410, the nickel element in the film is removed as much as possible. Furthermore, the crystalline silicon film 410 has high crystallinity by the effect of nickel. This crystalline silicon film becomes an active layer for TFTs later.

[0131]

Next, the mask 406 formed of the silicon oxide film is removed. Then, a mask for doping (not shown) is provided to selectively perform phosphorus doping into the active layer.

[0132]

In this step, phosphorus is doped into regions 411 and 413. Note that in this embodiment, an example of a case where an N-channel TFT is manufactured is shown. However, if a P-channel TFT is manufactured, boron doping may be performed.

[0133]

After doping, laser annealing is carried out to activate the doped regions.

[0134]

In this manner, the source region 411, a channel region 412, and the drain region 413 are formed. (FIG. 4 (D))

[0135]

Next, a silicon nitride film 414 is formed as an interlayer insulating film with a thickness of 300 nm by plasma CVD. Furthermore, an acrylic resin film 415 is formed by spin coating.

[0136]

Besides the acrylic resin film, a resin material such as polyimide, polyamide, polyimide amide, and epoxy can be used.

[0137]

After forming the interlayer insulating film, a contact hole is formed to form a source electrode 416 and a drain electrode 417. In this way, a bottom-gate TFT is completed shown in FIG. 4 (D).

[0138]

[Embodiment 6]

In this embodiment, examples of integrated circuits using TFTs are shown. As the examples of integrated circuits, a CPU, a memory, various arithmetic circuits, an amplifier circuit, a switch circuit and the like can be cited. A schematic view of an integrated circuit using TFTs and a cross-sectional view of a part thereof are shown in FIG. 5.

[0139]

[Embodiment 7]

A thin film transistor disclosed in this specification can be used in various flat-panel displays, an information processing terminal, a video camera and the like with a flat-panel display. In this specification, these apparatus are collectively referred to as semiconductor devices.

[0140]

Examples of specific configuration of various devices are hereinafter described. Examples of various semiconductor devices are described in FIG. 6. These semiconductor devices use TFTs in at least one part thereof.

[0141]

A portable information processing terminal is shown in FIG. 6 (A). This

information processing terminal includes an active matrix liquid crystal display or an active matrix EL display in a main body 2001 and provides a camera portion 2002 for receiving information from outside. Moreover, an integrated circuit 2006 is incorporated inside the body.

[0142]

An image reception portion 2003 and an operation switch 2004 are arranged in the camera portion 2002.

[0143]

It is considered that information processing terminals will be made thinner and lighter from now on to improve portability thereof.

[0144]

In such a structure, a peripheral driver circuit, an arithmetic circuit, and a memory circuit are preferably integrated by TFTs over a substrate over which an active matrix display 2005 is formed.

[0145]

A head-mounted display is shown in FIG. 6 (B). This apparatus includes an active matrix liquid crystal display or an EL display 2102 for a main body 2101. Moreover, the main body 2101 can be mounted on a head with a band 2103.

[0146]

Shown in FIG. 6 (C) is a car navigation system which receives a signal from an artificial satellite at an antenna 2204 and functions to display geographic information based on the signal on an active matrix liquid crystal display 2202 provided in a main body 2201.

[0147]

An EL display device can be adopted as the display 2202. In either case, the display is an active matrix flat-panel display using TFTs.

[0148]

Further, the main body 2201 includes operation switches 2203 to perform various operations.

[0149]

A cellular phone is shown in FIG. 3 (D). This apparatus includes an active matrix liquid crystal display device 2304, operation switches 2305, a sound input portion 2303, a sound output portion 2302 and an antenna 2306 in a main body 2301.

[0150]

Moreover, in recent years, a configuration with a combination of the portable information processing terminal shown in (A) and the cellular phone shown in (D) has also been commercialized.

[0151]

A portable video camera is shown in FIG. 3 (E). The portable video camera includes an image reception portion 2406, a sound input portion 2403, operation switches 2404, an active matrix liquid crystal display 2402 and a battery 2405 in a main body 2401.

[0152]

A rear projection liquid crystal display device is shown in FIG. 3 (F). This configuration includes a screen for projection in a main body 2501. A display is that light from a light source 2502 is divided by a polarizing beam splitter 2504, the divided light is optically modulated by a reflective liquid crystal display device 2503, reflectors 2505 and 2506 reflect the optically modulated image, and the optically reflected image is projected on a screen 2507.

[0153]

Here, an example using a reflective type is described as the liquid crystal display device 2503. However, a transmissive liquid crystal display device may also be used herein. In this case, an optical system may be changed.

[0154]

Moreover, examples of the liquid crystal displays are mainly described here, though an EL display device may be adopted as the active matrix display device.

[0155]

[Effect of the Invention]

By adopting the invention disclosed in this specification, a configuration can be provided which eliminates an effect of a nickel element remaining in an obtained silicon

film in a technique for obtaining a crystalline silicon film using a metal element for promoting crystallization of silicon.

[0156]

That is, a TFT using a silicon film having high crystallinity can be manufactured. Further, the effect of the metal element by the TFT can be decreased.

[0157]

In the invention disclosed in this specification, since the configuration to form a thin film for gettering the metal element is adopted, relatively simple and high productivity can be obtained.

[Brief Description of the Drawings]

FIG. 1 shows diagrams showing manufacturing steps of a TFT.

FIG. 2 shows diagrams showing manufacturing steps of a TFT.

FIG. 3 shows diagrams showing manufacturing steps of a TFT.

FIG. 4 shows diagrams showing manufacturing steps of a TFT.

FIG. 5 is a diagram showing a part of an integrated circuit using a TFT.

FIG. 6 are views each showing an outline of a device using a TFT.

[Description of the Numerals]

101: glass substrate, 100: base film (silicon oxide film), 102: amorphous silicon film, 103: nickel element maintained in contact with a surface, 104: crystalline silicon film, 105: mask formed of a silicon oxide film, 106: amorphous silicon film doped with phosphorus at high concentration, 107: patterned crystalline silicon film, 108: silicon oxide film (gate insulating film), 109: aluminum film pattern, 200: resist mask, 110: gate electrode (remaining aluminum pattern), 111: porous anodic oxide film, 112: anodic oxide film having dense membranous, 113: remaining silicon oxide film (gate insulating film), 114: high concentration impurity region (source region), 115: undoped region, 116: high concentration impurity region (drain region), 201: low concentration impurity region, 202: channel region, 203: low concentration impurity region, 204: silicon nitride film (interlayer insulating film), 117: acrylic resin film, 118: source electrode, 119: drain electrode

[Document Name] Abstract

[Summary]

[Problem] To remove nickel out of a silicon film which is crystallized by using nickel.

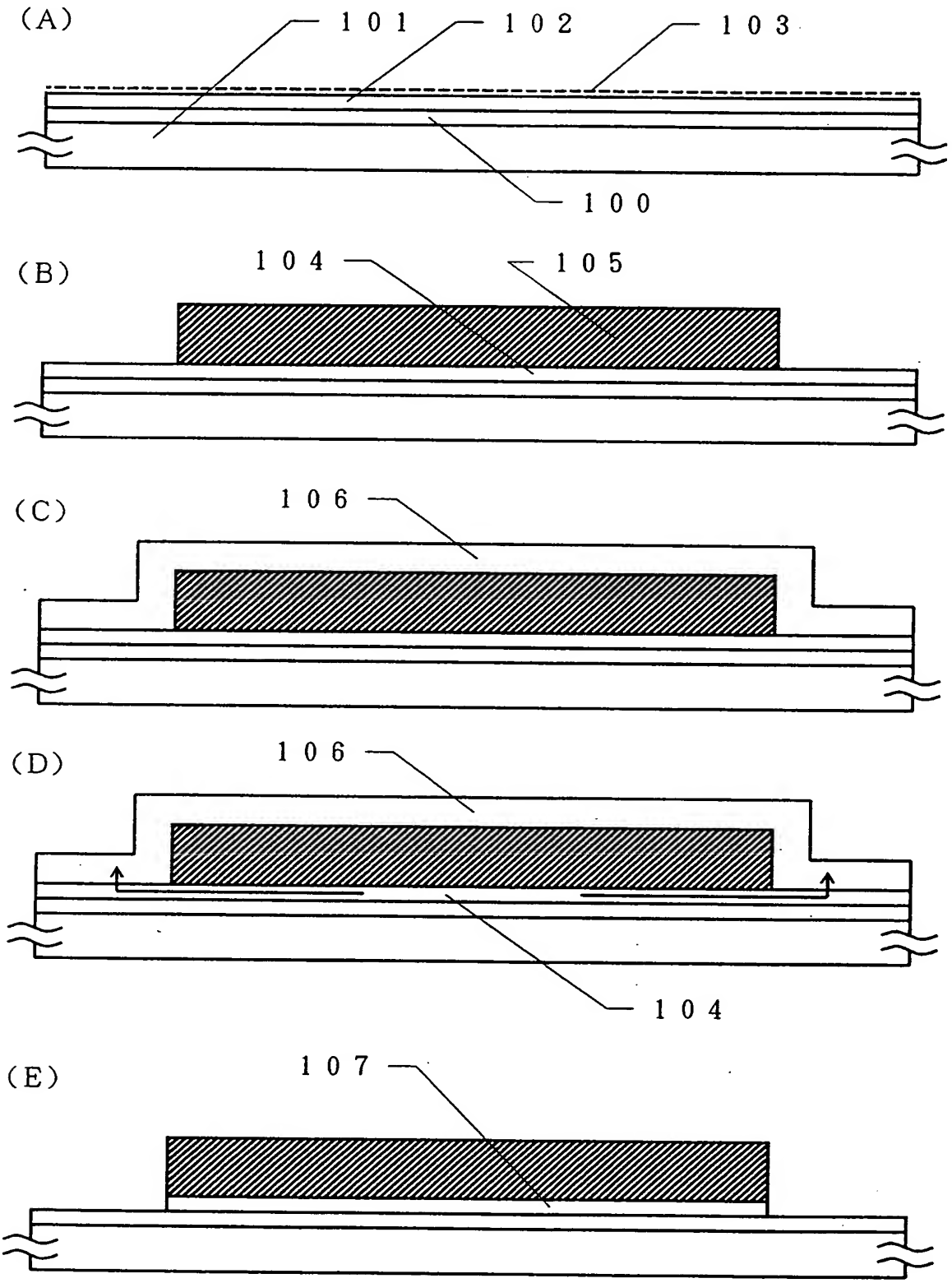
[Solving Means] A nickel element is maintained in contact with a surface of an amorphous silicon film 102 as indicated by reference numeral 103. Then, a crystalline silicon film 104 is obtained by heat treatment. At this time, an effect of the nickel element significantly promotes crystallization. Moreover, at the crystallization, the nickel element is diffused into the film. Then, a mask 105 is formed, furthermore, a silicon film 106 containing phosphorous at high concentration is formed. Then, by performing heat treatment, the nickel element in the crystalline silicon film 104 is moved into the silicon film 106. In this way, nickel concentration in the crystalline silicon film 104 is decreased.

[Selected Drawing] FIG. 1

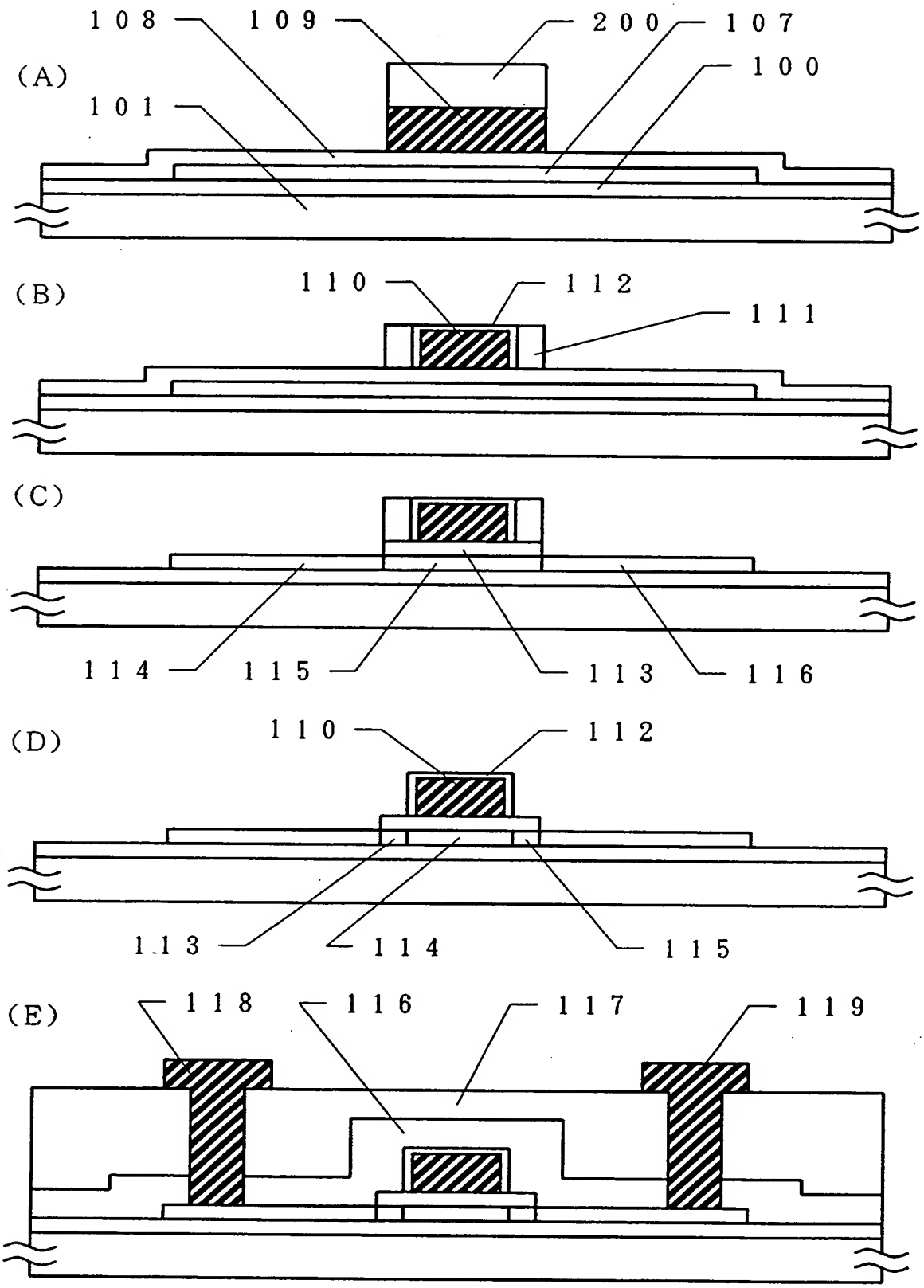
[Reference Number] P003674-02

[Name of document] Drawing

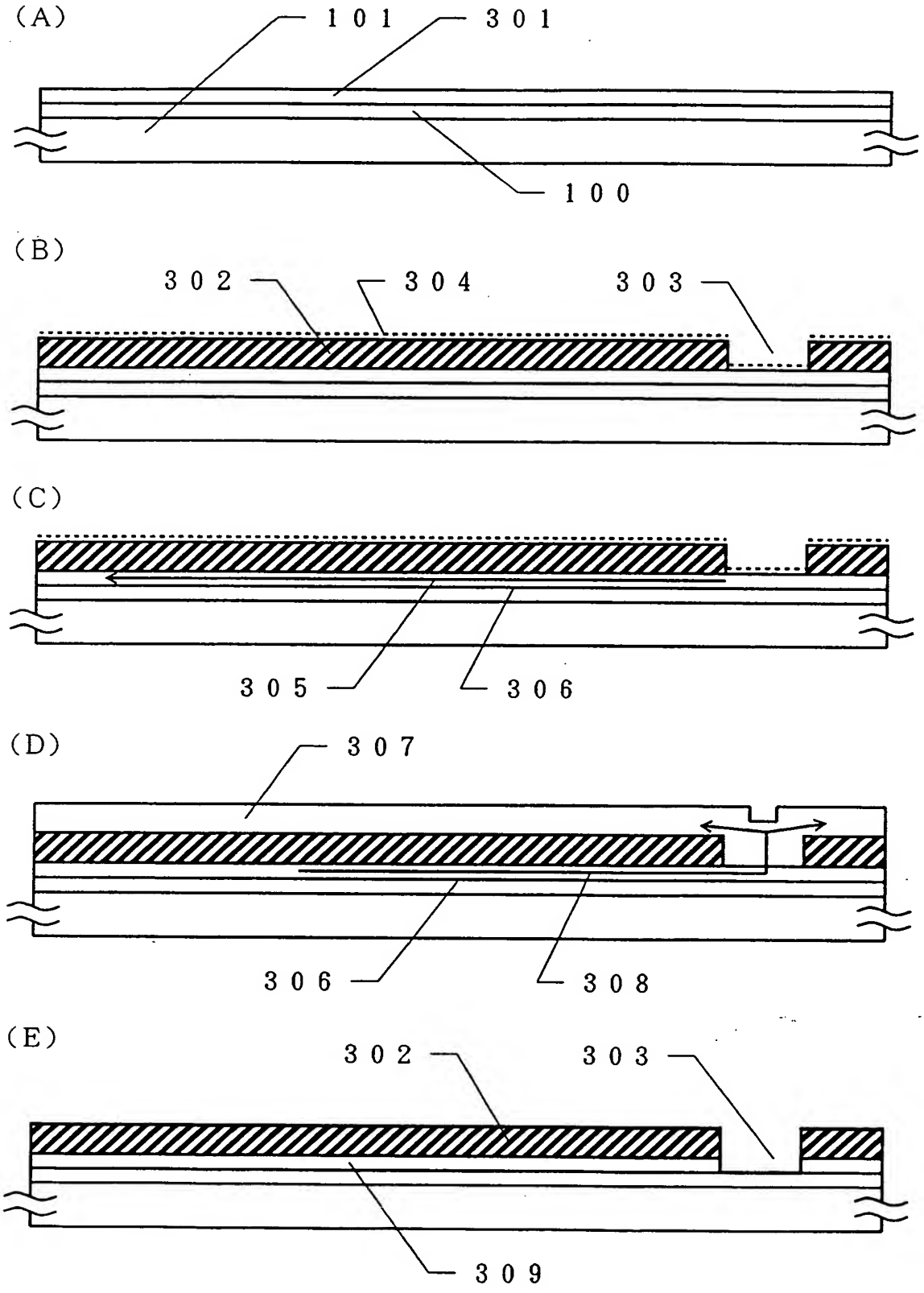
[FIG. 1]



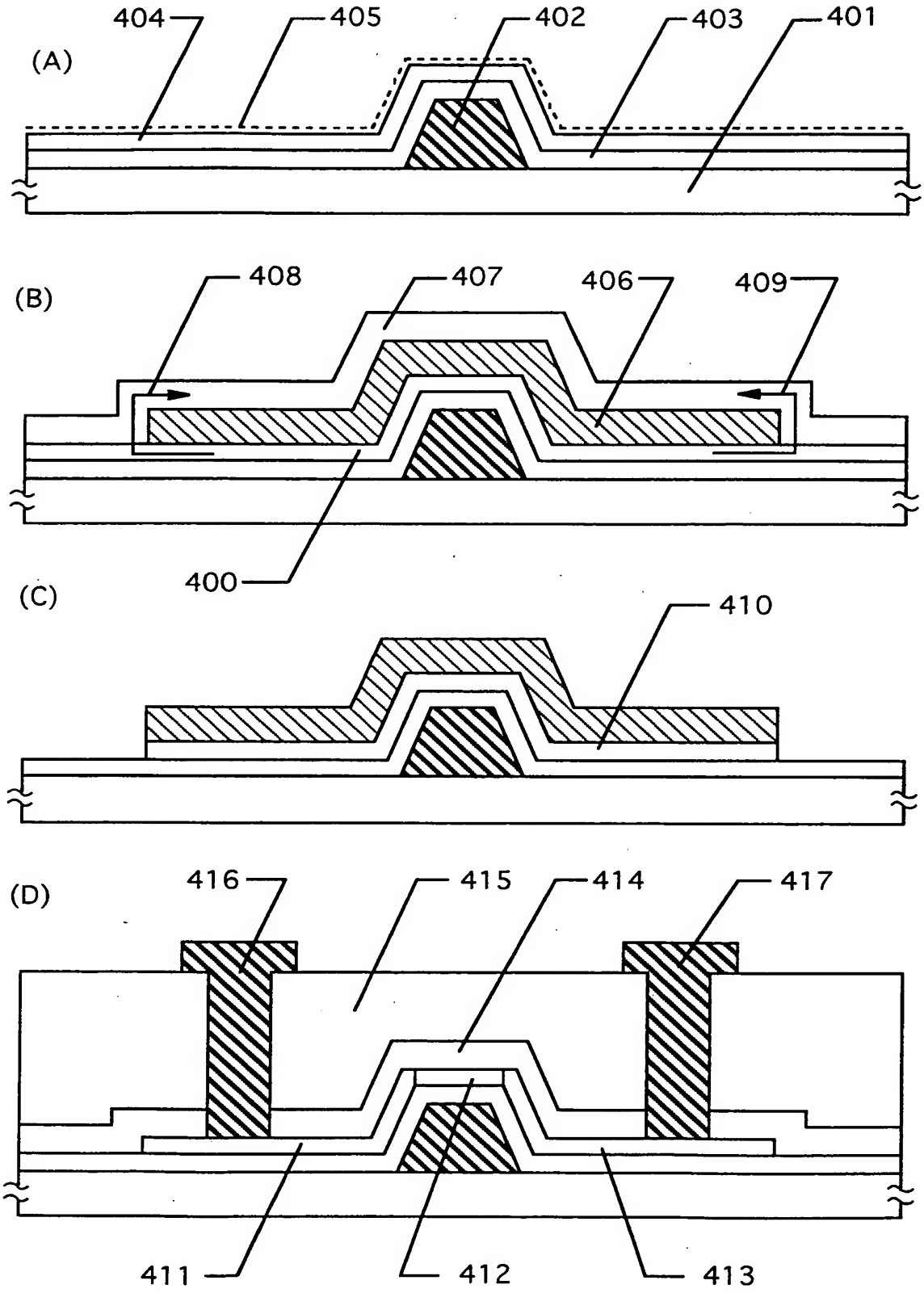
[FIG.2]


(A)
108
109
200
107
100
101
(B)
110
112
111
(C)
114
115
113
116
(D)
110
112
113
114
115
(E)
118
116
117
119

[FIG.3]



[FIG.4]


(A)
404
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(C)
410
(D)
416
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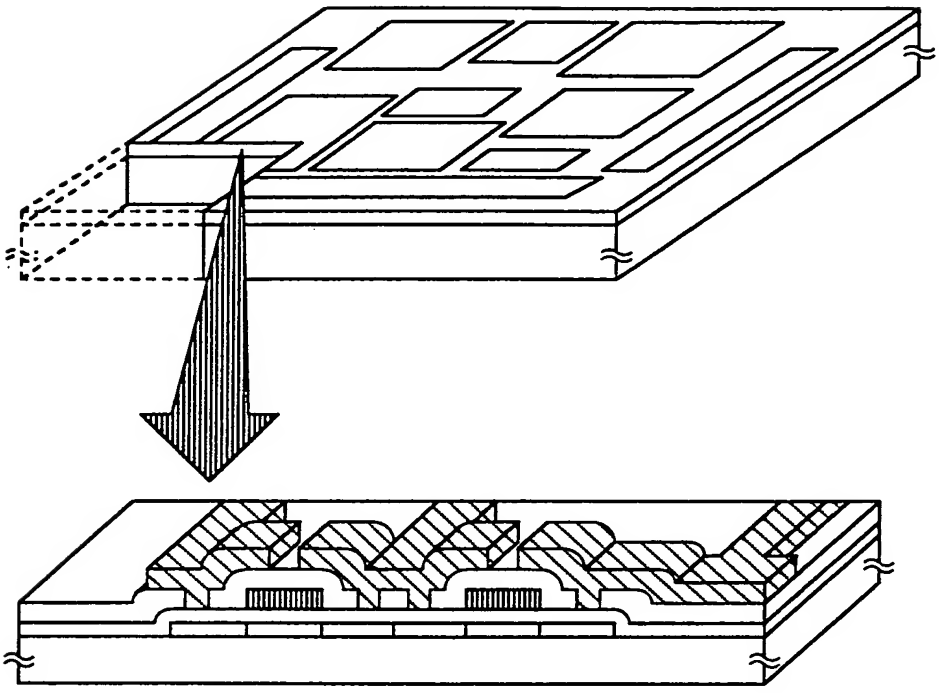
412
413

[Reference Number] P.003674-02

[FIG. 5]



[Reference Number] P003674-02

[FIG. 6]